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09/303,669	05/03/1999	STEFANOS SIDIROPOULOS	RMBS.002	8670

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EXAMINER	
FAN, CHIEH M	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 04/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/303,669	SIDIROPOULOS, STEFANOS	
	Examiner	Art Unit	
	Chieh M Fan	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10,11 and 26-29* is/are rejected.

7)☒ Claim(s) *5-9,12-25,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: logic NAND gate 607 (see page 17, line 9). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 5-9, 11-15, 17-25 and 31 are objected to because of the following informalities:

Regarding claims **5-9**, claim 5 recites the limitations of "a third supply voltage" and "a fourth supply voltage", but never recites a first supply voltage and a second supply voltage. Therefore, the following changes should be made:

(1) In claim 5, lines 3-4, "a third supply voltage" should be changed to "a first supply voltage";

(2) In claim 5, line 5, "a fourth supply voltage" should be changed to "a second supply voltage";

(3) In claim 6, line 1, "a second load" should be "the second load";

(4) In claim 6, line 3, "the third supply voltage" should be changed to "the first supply voltage";

(5) In claim 6, lines 3-4, "the fourth supply voltage" should be changed to "the second supply voltage";

(6) In claim 8, line 4, "the first and second load transistor" should be "the first and second load transistors";

(7) In claim 8, lines 4-5, "a fifth supply voltage" should be changed to "a third supply voltage";

(8) In claim 8, lines 6-7, "a sixth supply voltage" should be changed to "a fourth supply voltage";

(9) In claim 8, lines 9-10, "the sixth supply voltage" should be changed to "the fourth supply voltage";

(10) In claim 9, line 3, "the fifth supply voltage" should be changed to "the third supply voltage";

(11) In claim 9, line 3, "the sixth supply voltage" should be changed to "the fourth supply voltage";

Regarding claim **11**, the examiner suggests the following changes to improve the readability.

(1) In line 3, "a logic gate" should be changed to "a first logic gate";

(2) In line 3, "the logic gate" should be changed to "the first logic gate";

(3) In line 5, "a logic gate" should be changed to "a second logic gate";

(4) In line 5, "the logic gate" should be changed to "the second logic gate".

Regarding claims **12-15**, the limitation "a supply voltage" in line 3 of claim 12 should be changed to "a first supply voltage", since the limitation "a supply voltage" has been used to represent the voltage input to the delay line in claim 1 (see line 3 of claim 1). Similarly, "the supply voltage" in lines 9 and16 of claim 12 and in line 1 of claim 13 should be changed to "the first supply voltage".

Regarding claims **17-25**, claims 17-25 recite the limitations "a first supply voltage", "a third supply voltage", "a fourth supply voltage", "a fifth supply voltage", "a sixth supply voltage", but never recite a second supply voltage. The examiner suggests changing the limitation "a supply terminal" in the last line of claim 17 to "a second supply voltage" to fill the gap. Otherwise, the applicant needs to change "a third supply voltage" to "a second supply voltage", "a fourth supply voltage" to "a third supply voltage", and so forth. Furthermore, the following informalities need to be changed:

(1) In claim 17, line 15, "a non-inverting" should be changed to "an inverting";

(2) In claim 17, line 21, "a bias voltage" should be "the bias voltage";

(3) In claim 19, lines 3-4, "the fourth supply voltage is a ground voltage" should be changed to "a fourth supply voltage coupled to the bias transistor, wherein the fourth supply voltage is a ground voltage" to provide a proper antecedent basis for "the fourth supply voltage";

(4) In claim 20, lines 1-2, "the first load transistor" should be "the first transistor";

(5) In claim 20, line 2, "the second load transistor" should be "the second transistor";

(6) In claim 20, line 3, "the first and second load transistor" should be changed "the first and second transistors";

(7) In claim 22, line 4, "the second current mirror" should be "the second current mirror load circuit";

(8) In claim 22, line 7, "the third load transistor" should be "the first load transistor";

(9) In claim 22, line 10, "the fourth load transistor" should be "the second load transistor";

(10) In claim 24, line 3, "the second current mirror bias" should be changed to "a second current mirror bias".

Regarding claim **31**, the limitation "having an output" in line 2 should be changed to "having a first input, a second input, and an output" to provide proper antecedent basis for the limitations of "the first input" and "the second input" in line 4 and line 5, respectively. Further, "the bias voltage" in line 7 should be changed to "the bias signal".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter).

Regarding claim **26**, Tamura discloses a method of generating a supply voltage ("CS" in Fig. 44, note that CS is a control voltage, see bottom of Fig. 45) for use in clock compensation circuitry (301 in Fig. 44), the clock compensation circuitry includes a plurality of delay elements in a delay line (311 in Fig. 4) and receives a clock signal ("CKr" in Fig. 44), the method comprising:

providing a supply voltage to a common source electrode of the plurality of delay elements ("CS" input to 311 in Fig. 44, also see Fig. 45 for the details of each of the delay element "D");

providing a delayed clock signal using the delay line ("CKin" in Fig. 44) , the delayed clock signal having a time delay with respect to the clock signal (as shown in Fig. 44, "CKin" is obtained by delaying "CKr");

detecting a delay skew between the delayed clock signal and the clock signal (312 in Fig. 44);

converting the delay skew to a voltage signal wherein the voltage signal is proportional to the delay skew (131 in Fig. 44, especially "Vco" output from 131 in Fig. 44); and

tracking the voltage signal using an amplifier (132 in Fig. 44) to generate the supply voltage ("CS" in Fig. 44).

Regarding claim **27**, Tamura also teaches that the delayed clock signal ("CKin" in Fig. 44) is provided by propagating the clock signal ("CKr" in Fig. 44) through the plurality of delay elements ("D" within 311 in Fig. 44) and tapping an output of one of the delay elements from the plurality of delay elements ("CKin" is output from the last delay element of 311 in Fig. 44).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Lai (US Patent 5,339,009).

Regarding claim **1**, Tamura discloses a clock alignment circuit comprising:

a delay line having a plurality of delay elements (311 in Fig. 44), wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage ("CS" input to 311 in Fig. 44, also see Fig. 45 for the details of each of the delay element "D", also note that "CS" is a control voltage, see bottom of Fig. 45), to generate a delayed clock signal ("CKin" in Fig. 44) with respect to a reference clock signal ("CKr" in Fig. 44);

a comparator (312 in Fig. 44), coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information ("UP" and "DN" output from 312 in Fig. 44), wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry (131 in Fig. 44), coupled to the comparator, to convert the delay differential information to a control signal ("Vco" output from 131 in Fig. 44), wherein the control signal is proportional to the delay differential information;

an amplifier (132 in Fig. 44) coupled to the charge pump circuitry, wherein the amplifier includes:

a first input ("+" terminal of 132 in Fig. 44) to receive the control signal;

a second input ("-" terminal of 132 in Fig. 44) to receive a feedback signal; and

an output (output of 132 in Fig. 44) to provide the supply voltage and the feedback signal.

Tamura does not teach a capacitor coupled between the supply voltage and a secondary power supply (i.e., a ground voltage).

However, the use of a capacitor to bypass or filter undesired high-frequency noise is known in the art. Lai teaches a capacitor (64 in Fig. 2) coupled to the output of an amplifier (54 in Fig. 2) and a secondary power supply to bypass or filter unwanted noise (col. 6, lines 19-23) of the signal output from the amplifier.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple a capacitor between the supply voltage and a secondary power supply in the circuit of Tamura to bypass or filter the undesired noise in the supply voltage before the supply voltage is supplied to the delay elements of the delay line, and consequently to generate a more stable delayed clock signal from the delay line.

Regarding claim **2**, Tamura teaches the claimed limitation that the first input is a non-inverting input (see "+" terminal of 132 in Fig. 44) and the second input is an inverting input (see "-" terminal of 132 in Fig. 44).

Regarding claim **4**, Tamura teaches the claimed limitation that the delay line includes a plurality of inverter delay elements (Fig. 45 and col. 32, lines 47-48).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. in view of Lai as applied to claim 1 above, and further in view of Dally et al. (*Digital Systems Engineering*, Cambridge, 1998, pp. 589-607).

As applied to claim 1 above, Tamura in view of Lai discloses the claimed invention including each of the delay elements in the delay line is an inverter delay element (col. 32, lines 47-48), but fails to disclose that the delay line includes a plurality of differential delay elements.

However, Dally et al. teaches that a differential delay element has better supply-noise rejection than an inverter delay element (the last two lines on page 593 through the first four lines on page 594).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the inverter delay elements in the delay line of Tamura in view of Lai with differential delay elements, since the use of differential delay elements has the advantage of higher power supply noise immunity than the use of inverter delay elements.

9. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. in view of Lai as applied to claim 1 above, and further in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Tamura in view of Lai teaches the claimed invention, as applied to claim 1 above, but fails to teach that the comparator includes a first pulse generator, a second pulse generator and a latch circuit as recited in claims 10 and 11, wherein the comparator corresponds to the comparator shown in Fig. 6 of the instant application. The first pulse generator corresponds to element 601 in Fig. 6. The second pulse generator corresponds to element 602 in Fig. 6. The latch circuit corresponds to element 603 in Fig. 6.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). The phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the reference clock signal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al.

in place of the phase comparator of Tamura in view of Lai, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

10. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Regarding claim **28**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, setting a latch circuit using the first pulse, and resetting the latch circuit using the second pulse, wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 601 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 602 in Fig. 6. The step of setting a latch circuit using the first pulse is achieved by sending the pulse 610 to the latch circuit 603. The step of resetting the latch circuit using the second pulse is achieved by sending the pulse 611 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle

imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 28.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Regarding claim **29**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, resetting a latch circuit using the first pulse, and setting the latch circuit using the second pulse, wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 602 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 601 in Fig. 6. The step of resetting a latch circuit using the first pulse is achieved by sending the pulse 611 to the latch circuit 603. The step of setting the latch

circuit using the second pulse is achieved by sending the pulse 610 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 29.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Allowable Subject Matter

11. Claims 5-9, 12-15, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims and rewritten to overcome the claim objections in Paragraph 3 of this Office Action.

12. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 17-25 would be allowable if rewritten or amended to overcome the claim objections in Paragraph 3 of this Office action.

14. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5-9 are allowable over the prior art of record because the prior art of record does not teach or suggest that the amplifier includes a current mirror load, a bias transistor, a first differential input transistor and a second differential input transistor.

Claims 12-15 are allowable over the prior art of record because the prior art of record does not teach or suggest that the charge pump circuitry includes a second current source receiving the first supply voltage, the second current source having a control electrode to receive the bias control signal, a second load transistor coupled to the first reference terminal, wherein the second load transistor responds to the first pump output; and a second input transistor coupled in series between the second

current source and the second load transistor, the second input transistor responsive to a second phase input to provide a charge pump output.

Claim 16 is allowable over the prior art of record because the prior art of record does not teach or suggest that the supply voltage is provided to the multiplexer circuit and the interpolation circuit.

Claims 17-25 are allowable over the prior art of record because the prior art of record does not teach or suggest the operational amplifier includes a bias transistor biased by a bias voltage, and a bias generator to provide the bias voltage, wherein the bias generator having a first input coupled to the control signal and a second input to receive the bias voltage.

Claims 30 and 31 are allowable over the prior art of record because the prior art of record does not teach or suggest that the step of tracking the voltage signal includes amplifying a voltage differential between the first input and the second input, biasing the current source with a bias signal, and generating the supply voltage at the output, wherein the supply voltage is proportional to the voltage differential.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dally et al. (US Patent 6,316,987) teaches a low-jitter variable delay timing circuit. Thoma et al. (US Patent 5,672,991) teaches a differential delay line circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Chieh M Fan
Examiner
Art Unit 2634

cmf
April 12, 2002